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(54) **ANALOG-TO-DIGITAL CONVERTER**

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(71) Applicant: **Telefonaktiebolaget L M Ericsson (publ)**, Stockholm (SE)

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(72) Inventors: **Martin Anderson**, Löddeköpinge (SE);
Lars Sundström, Södra Sandby (SE)

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(73) Assignee: **Telefonaktiebolaget L M Ericsson (publ)**, Stockholm (SE)

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H03M 7/3022; H03M 7/3042; H03K 3/0231
USPC 341/143–155; 375/243, 247; 327/552
See application file for complete search history.

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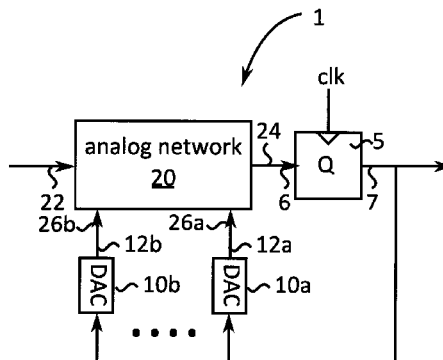
(74) Attorney, Agent, or Firm — Murphy, Bilak & Homiller, PLLC

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ABSTRACT

A continuous-time $\Delta\Sigma$ -ADC (1) is disclosed, comprising a sampled quantizer (5) arranged to generate samples $y(n)$ of a digital output signal of the $\Delta\Sigma$ -ADC (1) at sample instants nT . The $\Delta\Sigma$ -ADC (1) further comprises two or more DACs (10a-b), each arranged to generate an analog feedback signal based on the samples of the digital output signal generated by the sampled quantizer (5), and a continuous-time analog network (20) arranged to generate an analog input signal to the quantizer (5) based on the feedback signal(s) from the two or more DACs (10a-b) and an analog input signal to the $\Delta\Sigma$ -ADC (1). At least a first DAC (10a) of the two or more DACs (10a-b) is adapted to generate a pulsed feedback signal that, for each n , comprises a pulse, the magnitude of which is proportional to the sample of the digital output signal at sample instant nT and which lasts between the time instants $(n+a_1)T$ and $(\eta+\beta_1)T$, wherein $0 < a_1 < \beta_1 < 1$. At least a second DAC (10b) of the two or more DACs (10a-b) is adapted to generate a pulsed feedback signal that, for each n , comprises a pulse, the magnitude of which is proportional to the sample of the digital output signal at sample instant nT and which lasts between the time instants $(n+a_2)T$ and $(\eta+\beta_2)T$, wherein $0 < a_2 < \beta_2 < 1$. The first DAC (10a) is located in a first feedback loop and the second DAC (10b) is located in a second feedback loop, which is an outer feedback loop relative to the first feedback loop. A corresponding radio receiver circuit, a corresponding integrated circuit, and a corresponding radio communication apparatus are also disclosed.

17 Claims, 6 Drawing Sheets



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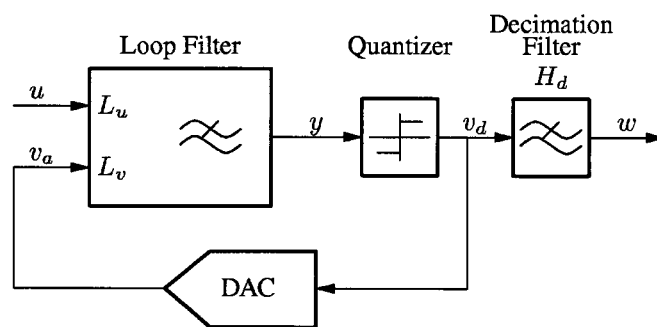


FIG. 1

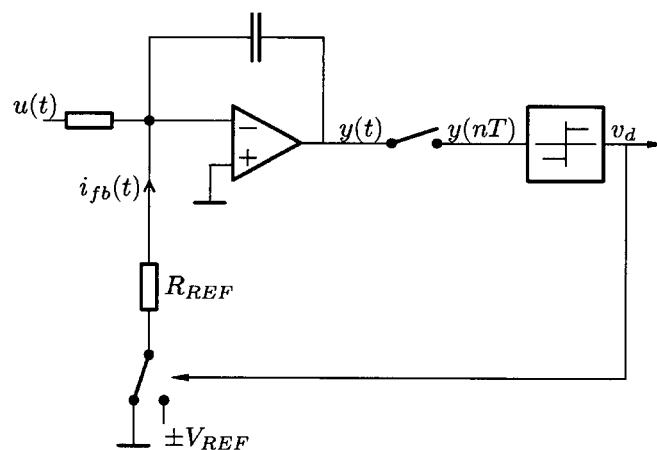


FIG. 2

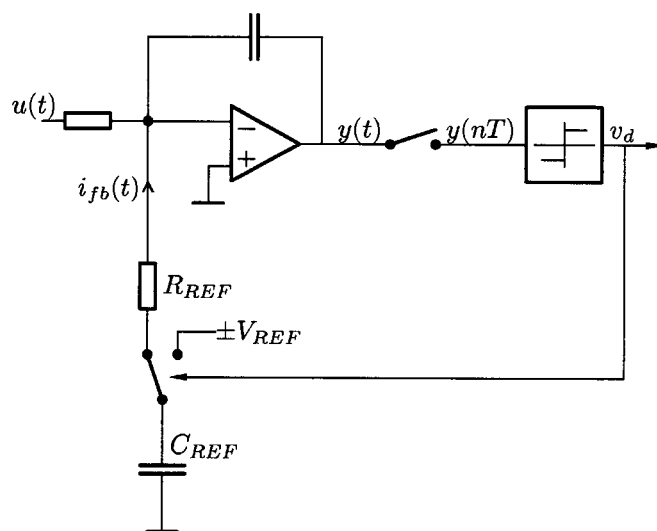


FIG. 3.

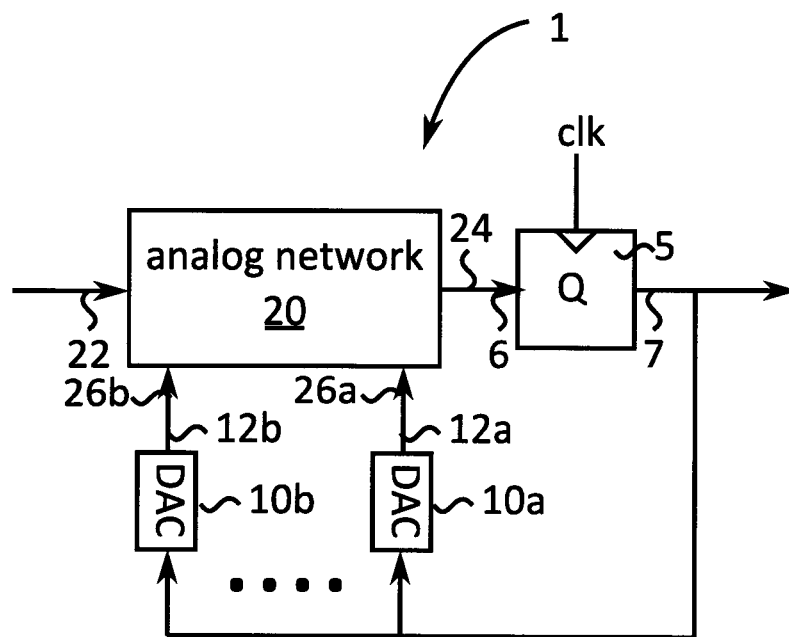


FIG. 4

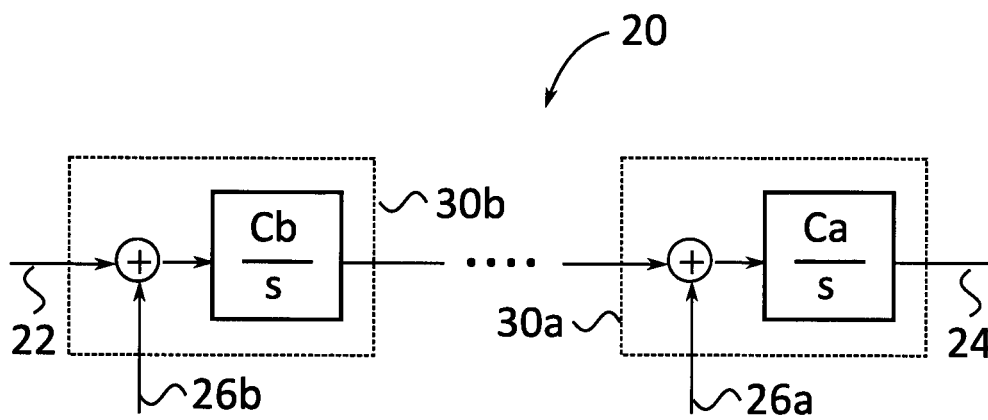


FIG. 5.

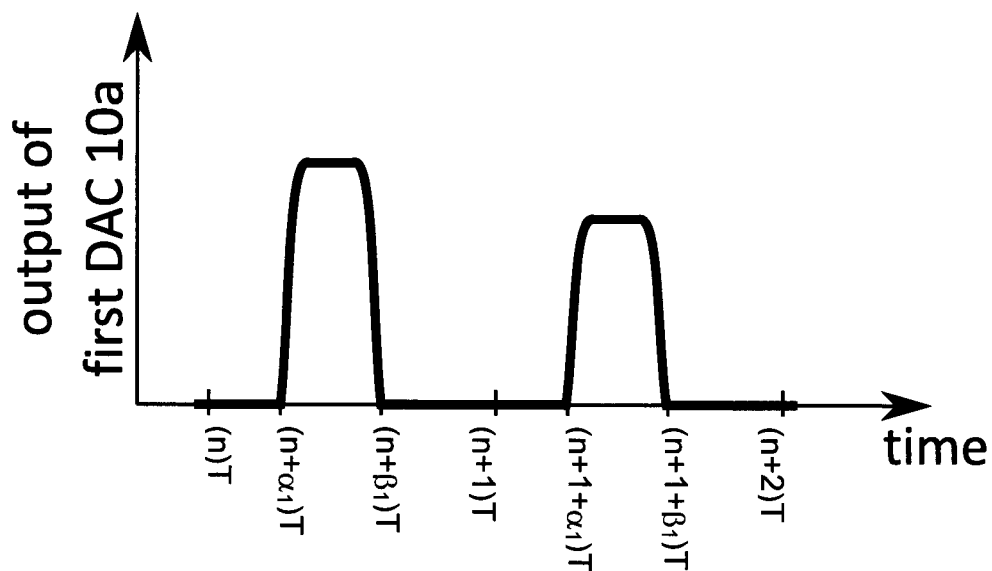


FIG. 6

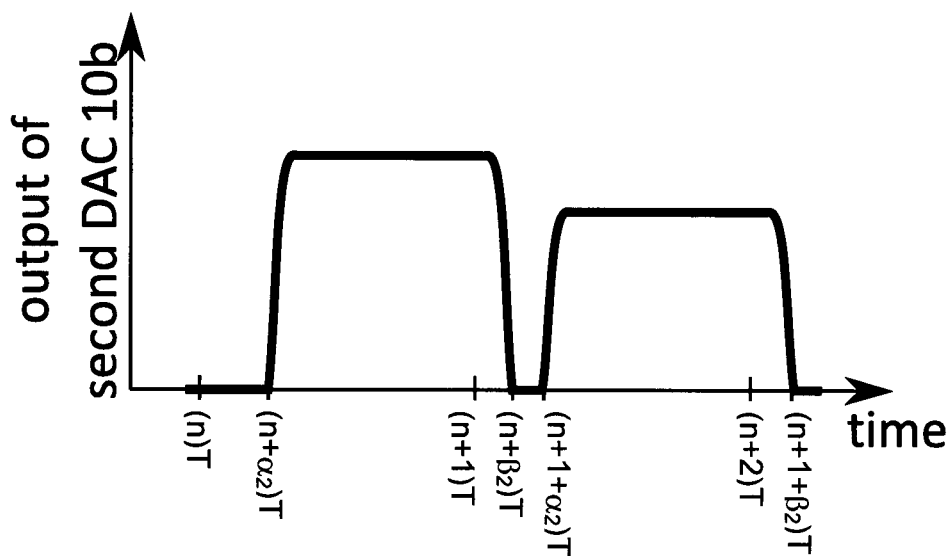


FIG. 7

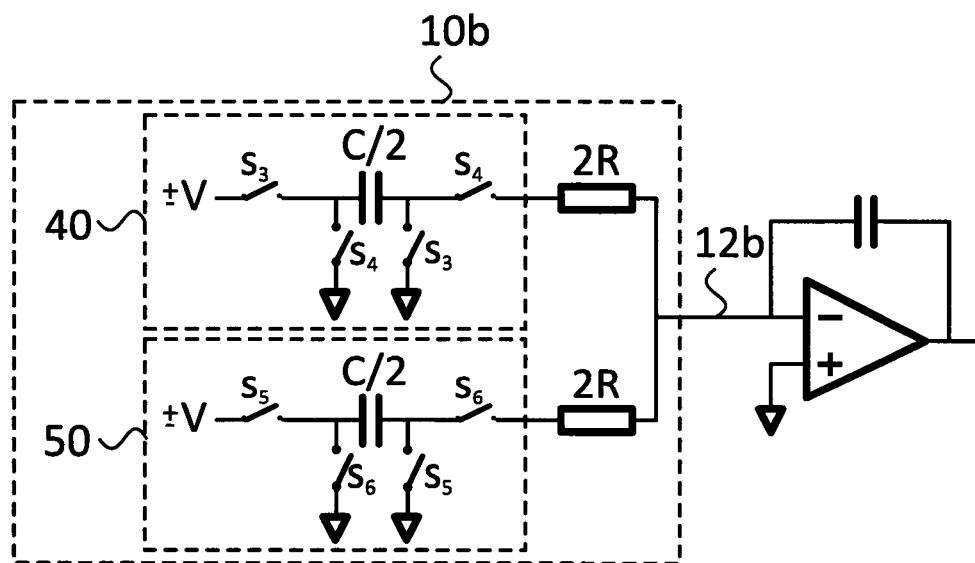


FIG. 8

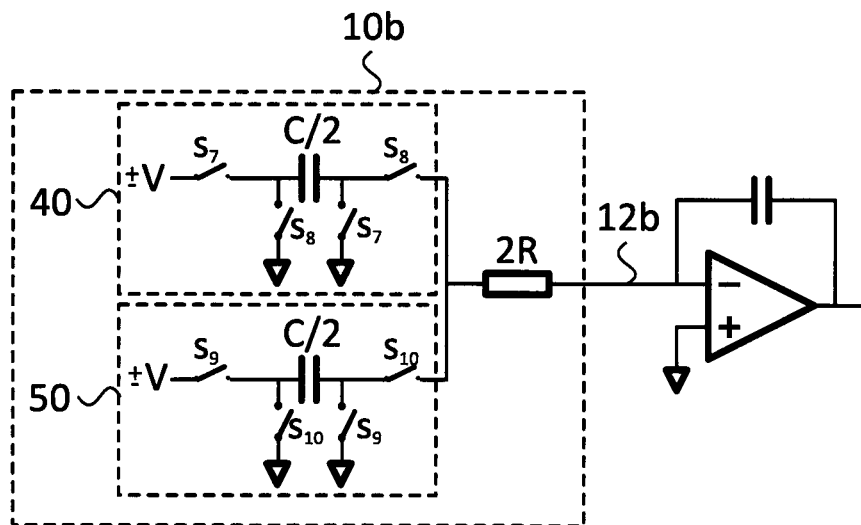


FIG. 9

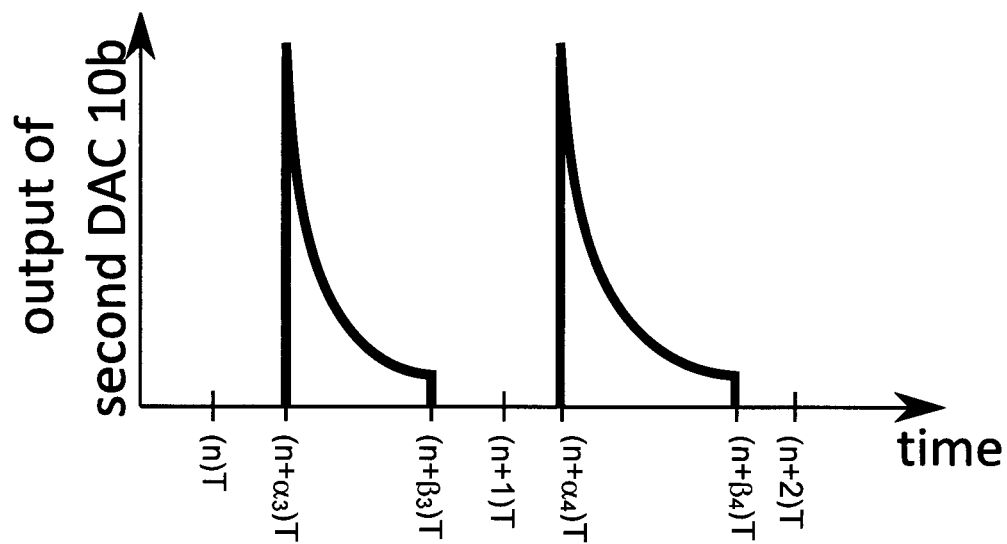


FIG. 10

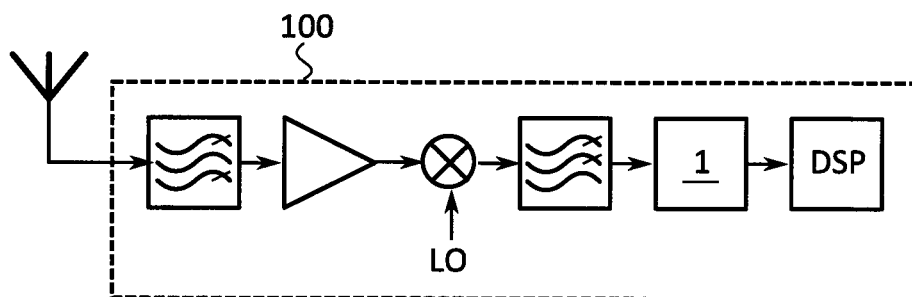


FIG. 11

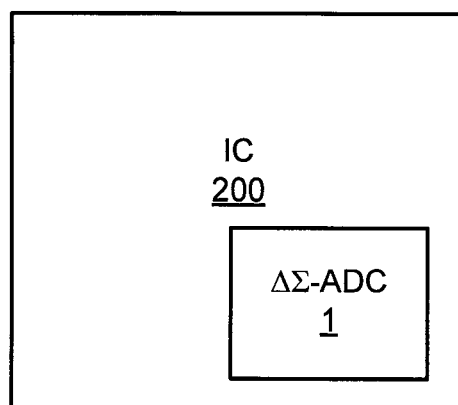


FIG. 12

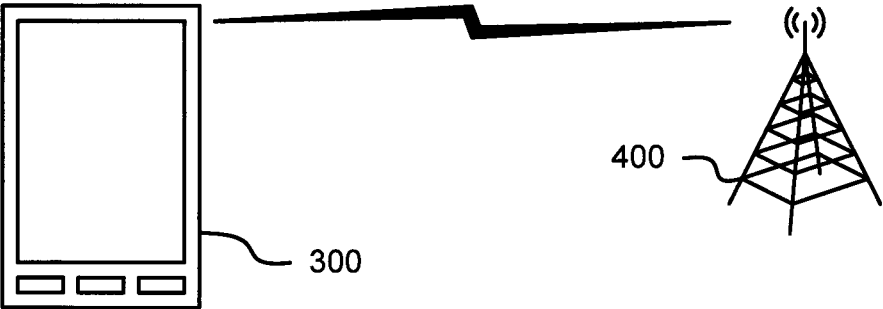


FIG. 13

ANALOG-TO-DIGITAL CONVERTER

TECHNICAL FIELD

The present invention relates to the field of analog-to-digital converters, in particular to the field of continuous-time delta-sigma analog-to-digital converters.

BACKGROUND

FIG. 1 shows a general depiction of a continuous-time delta sigma ($\Delta\Sigma$) analog-to-digital converter (ADC). The conventional $\Delta\Sigma$ ADC converts an analog input signal u into a high-frequency serial bit sequence having a low resolution, often only 1 bit (0 or 1), here called v_d . This coarsely quantized bit sequence v_d is converted into a highly accurate digital signal w with a lower sampling rate through subsequent digital low pass decimation filters, H_d . This is possible since the energy of the quantization noise is distributed at frequencies outside the frequency band of interest.

The $\Delta\Sigma$ ADC of FIG. 1 comprises a coarse quantizer, a loop filter and a feedback DAC. The coarse quantizer comprises one or more comparators clocked at a clock rate a lot higher than the bandwidth of the analog input signal u . The digital-to-analog converter (DAC) provided in the feedback branch generates from the digital output signal of the quantizer, v_d , a sequence of quantized analog signals here called the feedback signal, v_a . The loop filter processes both the analog input signal u and the quantization errors, ϵ , injected into the system in the coarse quantizer. By selecting the transfer function of the loop filter, L_u and L_v , in such a way that, in the band of interest, the transfer function for the quantization errors ϵ is many times smaller than the transfer function for the analog input signal u , the signal-to-quantization “noise” ratio (SQNR) in that particular frequency band can be made large.

Thus, by selecting L_v properly, the noise transfer function (NTF) can be made high-pass or band-pass:

$$NTF = \frac{v_d}{\epsilon} = \frac{1}{1 - L_v} \quad (1)$$

whereas the signal transfer function (STF) is a function of both L_u and L_v :

$$STF = \frac{v_d}{u} = \frac{L_u}{1 - L_v} \quad (2)$$

The loop filter can be implemented using active discrete time (DT) filters or active continuous time (CT) filters or even passive loop filters. If the NTF is selected having zeros at low frequencies (DC), the loop filter will be built up of integrators, which can be implemented using negative feedback amplifiers. The reason for using CT filters above their DT counterparts is that they provide anti-alias filtering, have no front-end sampling, no kT/C noise and theoretical speed advantages which lead to a lower power consumption at a given analog signal bandwidth.

Prior art in the implementation of the feedback DAC in CT modulators is to use a switched current (SI), or a switched capacitor (SC) to inject a well defined amount of charge to the summing node of the integrator.

FIG. 2 shows a possible implementation of a 1-bit SI feedback according to prior art. A logically high data bit of the digital output signal (HIGH), v_d , is applied as a correspond-

ing reference voltage (for example $V_{REF+}=1$ volt) to the inverting signal input of the amplifier, and a logically low signal (LOW) of the digital output signal is fed back as a second reference voltage (for example $V_{REF-}=-1$ volt). The reference voltage is converted to a reference current through the resistor between the V_{REF} node and the virtual ground (summing node) at the amplifier input.

In the SC feedback according to prior art (e.g. FIG. 3) a capacitor C_{REF} is switched using a set of switches between the reference voltage V_{REF} and to the inverting input of the operational amplifier. A reference resistance R_{REF} might be connected on either side of the capacitor to control the time constant of the switching RC circuit. The reference capacitor is charged with the reference voltage (V_{REF+} or V_{REF-}) corresponding to the digital output bit in a first clock phase, and then transfers a well defined charge packet $Q=C \cdot V_{REF}$ to the integrator in a second clock phase when the switch circuit switches the reference capacitor C_{REF} to the inverting input of the amplifier. The discharge of the capacitor C_{REF} will give an exponentially falling current pulse $I=I_0 \cdot \exp(-t/\tau)$ where $\tau=R_{REF} \cdot C_{REF}$ is the time constant. Because of the exponentially decreasing pulse shape the charge Q displaced in one clock cycle T varies only slightly when clock jitter occurs, and thus this technique is less sensitive to clock jitter than the $\Delta\Sigma$ ADCs illustrated in FIG. 2.

SUMMARY

In accordance with embodiments of the present invention, the inventors have provided for the design of continuous-time $\Delta\Sigma$ ADCs with relatively low sensitivity to clock jitter and loop delay.

According to a first aspect, there is provided a continuous-time delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC). The $\Delta\Sigma$ -ADC comprises a sampled quantizer arranged to generate samples $y(n)$ of a digital output signal of the $\Delta\Sigma$ -ADC at sample instants nT , where n is an integer sequence index and T is a sampling period, based on an analog input signal to the quantizer. The $\Delta\Sigma$ -ADC further comprises two or more digital-to-analog converters (DACs) each arranged to generate an analog feedback signal based on the samples of the digital output signal generated by the sampled quantizer. Moreover, the $\Delta\Sigma$ -ADC comprises a continuous-time analog network arranged to generate the analog input signal to the quantizer based on the feedback signals from the two or more DACs and an analog input signal to the $\Delta\Sigma$ -ADC. At least a first DAC of the two or more DACs is adapted to generate a pulsed feedback signal that, for each n , comprises a pulse, the magnitude of which is proportional to the sample of the digital output signal at sample instant nT and which lasts between the time instants $(n+\alpha_1)T$ and $(n+\approx 1)T$, wherein $0 < \alpha_1 < \beta_1 < 1$. Furthermore, at least a second DAC of the two or more DACs is adapted to generate a pulsed feedback signal that, for each n , comprises a pulse, the magnitude of which is proportional to the sample of the digital output signal at sample instant nT and which lasts between the time instants $(n+\alpha_2)T$ and $(n+\beta_2)T$, wherein $0 < \alpha_2 < 1 < \beta_2$. The first DAC is located in a first feedback loop and the second DAC is located in a second feedback loop, which is an outer feedback loop relative to the first feedback loop (i.e. a loop that has a higher order of integration than the first loop).

According to some embodiments, $\beta_1 < 0.9$, such as but not limited to $\beta_1 = 0.625$ or $\beta_1 = 0.75$.

According to some embodiments, $\alpha_1 > 0.1$, such as but not limited to $\alpha_1 = 0.125$ or $\alpha_1 = 0.25$.

According to some embodiments, $\beta_2 - \alpha_2 = 1$.

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According to some embodiments, at least one DAC of the two or more DACs comprises two switched-capacitor DACs. For each n , each of the two switched capacitor DACs may be arranged to be charged with a charge proportional to the corresponding sample $y(n)$ of the digital output signal. Furthermore, for each n , a first of the switched capacitor DACs may be arranged to be switched in to the continuous-time analog network for transfer of its charge to the continuous-time analog network in a time interval that lasts between the time instants $(n+\alpha 3)T$ and $(n+\beta 3)T$. Similarly, for each n , a second of the switched capacitor DACs may be arranged to be switched in to the continuous-time analog network for transfer of its charge to the continuous-time analog network in a time interval that lasts between the time instants $(n+\alpha 4)T$ and $(n+\beta 4)T$. The following relations may apply: $\beta 4 > 1$, $0 < \alpha 3 < \alpha 4 < \beta 4 < 2$ and $\alpha 3 < \beta 3 \leq 1$.

In some embodiments, the first DAC may be located in said first feedback loop and the DAC comprising the two switched capacitor DACs may be located in another feedback loop, which is an outer feedback loop relative to the first feedback loop. In some embodiments, the second DAC is the DAC that comprises the two switched-capacitor DACs.

The continuous-time analog network may comprise a plurality of cascaded continuous-time integrators. A first one of the integrators may be arranged to receive a feedback signal from one of the DACs, connected to the first integrator, and the analog input signal of the $\Delta\Sigma$ -ADC as input signals. Each of the other integrators may be arranged to receive a feedback signal from one of the DACs, connected to that integrator, and an output signal of a preceding integrator as input signals.

A last one of the cascaded continuous-time integrators may be arranged to generate the analog input signal to the sampled quantizer.

According to a second aspect, there is provided a radio receiver circuit comprising the continuous-time $\Delta\Sigma$ -ADC according to the first aspect.

According to a third aspect, there is provided an integrated circuit comprising the continuous-time $\Delta\Sigma$ -ADC according to the first aspect.

According to a fourth aspect, there is provided a radio communication apparatus comprising the continuous-time $\Delta\Sigma$ -ADC according to the first aspect, the radio receiver circuit according to the second aspect, and/or the integrated circuit according to the third aspect.

The radio communication apparatus may e.g. be, but is not limited to, a mobile phone, a wireless data modem, or a radio base station.

Further embodiments are defined in the dependent claims. It should be emphasized that the term "comprises/comprising" when used in this specification is taken to specify the presence of stated features, integers, steps, or components, but does not preclude the presence or addition of one or more other features, integers, steps, components, or groups thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

Further objects, features and advantages of embodiments of the invention will appear from the following detailed description, reference being made to the accompanying drawings, in which:

FIGS. 1-3 illustrate general continuous-time $\Delta\Sigma$ -ADCs; FIG. 4 illustrates a continuous-time $\Delta\Sigma$ -ADC according to embodiments of the present invention;

FIG. 5 illustrates a continuous-time analog network according to embodiments of the present invention;

FIGS. 6-7 illustrate examples of pulse waveforms;

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FIGS. 8-9 illustrate digital-to-analog converters (DACs) according to embodiments of the present invention;

FIG. 10 illustrates an example of pulse waveforms;

FIG. 11 schematically illustrates a radio receiver circuit;

FIG. 12 schematically illustrates an integrated circuit; and

FIG. 13 schematically illustrates a mobile phone in communication with a radio base station.

DETAILED DESCRIPTION

FIG. 4 is a simplified block diagram of a continuous-time delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC) 1 according to embodiments of the present invention. The $\Delta\Sigma$ -ADC 1 comprises a sampled quantizer 5. The sampled quantizer 5 is arranged to receive an analog input signal of the sampled quantizer 5 on an input terminal 6. The sampled quantizer 5 is arranged to generate samples of a digital output signal of the $\Delta\Sigma$ -ADC 1 at sample instants nT (where n is an integer sequence index and T is a sampling period of the clock signal clk), based on the analog input signal to the quantizer 5. The sample of the digital output signal at the sample instant nT is in the following denoted $y(n)$. The digital output signal is generated on an output port 7 of the sampled quantizer 5. The sampled quantizer 5 may be a single-bit or a multibit quantizer.

In addition, the $\Delta\Sigma$ -ADC 1 comprises two or more digital-to-analog converters (DACs) 10a-b, each arranged to generate an analog feedback signal based on the samples of the digital output signal generated by the sampled quantizer 5 on output terminals 12a-b. Each of said two or more DACs may e.g. be of switched-current (e.g. similar to the SI feedback discussed with reference to FIG. 2) or switched-capacitor (e.g. similar to the SI feedback discussed with reference to FIG. 3) type. Furthermore, the $\Delta\Sigma$ -ADC 1 comprises a continuous-time analog network 20. The continuous-time analog network 20 has an input terminal 26a-b for each of the two or more DACs 10a-b for receiving the feedback signals generated by the DACs 10a-b. The continuous-time analog network is arranged to generate the analog input signal to the quantizer 5, on an output terminal 24 of the continuous-time analog network 20, based on the feedback signals from the two or more DACs 10a-b and an analog input signal to the $\Delta\Sigma$ -ADC 1, received on an input terminal 22 of the continuous-time analog network 20.

An example of how the continuous-time analog network 20 may be embodied is illustrated in FIG. 5. As illustrated in FIG. 5, the continuous-time analog network 20 may comprise a plurality of cascaded continuous-time integrators 30a-b. A first one of the integrators (in FIG. 5, the integrator 30b) may be arranged to receive a feedback signal from one of the DACs connected to the first integrator 30b, and the analog input signal of the $\Delta\Sigma$ -ADC 1 as input signals. Furthermore, as illustrated in FIG. 5, each of the other integrators may be arranged to receive a feedback signal from one of the DACs, connected to that integrator, and the output signal of a preceding integrator as input signals. Moreover, as illustrated in FIG. 5, a last one of the cascaded continuous-time integrators (in FIG. 5, the integrator 30a) may be arranged to generate the analog input signal to the sampled quantizer 5. The integrators may e.g. be implemented as active RC integrators or Gm-C integrators. The design of such integrators with multiple inputs is well known and therefore not further described herein.

According to embodiments of the present invention, at least a first DAC (e.g. 10a, which is the reference sign used for the first DAC in the following) of the two or more DACs 10a-b is adapted to generate a pulsed feedback signal that, for each

n, comprises a pulse (e.g. output electrical current pulse), the magnitude of which is proportional to the sample of the digital output signal at sample instant nT and which lasts between the time instants $(n+\alpha_1)T$ and $(n+\beta_1)T$, wherein $0<\alpha_1<\beta_1<1$. This is schematically illustrated in FIG. 6 with a waveform diagram.

According to embodiments of the present invention, at least a second DAC (e.g. **10b**, which is the reference sign used for the second DAC in the following) of the two or more DACs **10a-b** is adapted to generate a pulsed feedback signal that, for each n, comprises a pulse, the magnitude of which is proportional to the sample of the digital output signal at sample instant nT and which lasts between the time instants $(n+\alpha_2)T$ and $(n+\beta_2)T$, wherein $0<\alpha_2<\beta_2<1$. This is schematically illustrated in FIG. 7 with a waveform diagram.

The inventors have realized that the inner loop or loops (loops with relatively low order of integration) of continuous-time $\Delta\Sigma$ -ADC contributes more to the sensitivity to excess loop delay of the $\Delta\Sigma$ -ADC, because their impact on the impulse response of the cascade of feedback DAC and loop filter is the largest, and therefore changes the loop gain of the system the most. The inventors have realized that using a DAC such as the aforementioned first DAC **10a** in such inner loop(s) alleviates this problem, since the impulse response of the cascade of feedback DAC and loop filter is less sensitive to a delay of such a feedback pulse. Thereby, the loop gain is affected less, making the closed loop performance of the $\Delta\Sigma$ -ADC more robust to such delays. In some embodiments, a memoryless feedback path may be included, i.e. with one DAC whose output contributes directly (i.e. without integration) to the analog input signal of the sampled quantizer. Referring to FIG. 5, the output of such a DAC would thus be added to the output of the integrator **30a** for forming the analog input signal to the sampled quantizer **5**. Such a memoryless path can provide a further reduced sensitivity to loop delay. In some embodiments, further feedback or feedforward paths may also be provided between internal nodes of the continuous-time analog network **20**.

In addition, the inventors have realized that the outer loop or loops (loops with relatively high order of integration) of continuous-time $\Delta\Sigma$ -ADC may be sensitive to clock jitter and thermal noise since such errors from the outermost loops have less noise shaping than the inner loops when referred to the output of the $\Delta\Sigma$ -ADC. The inventors have realized that using a DAC such as the aforementioned second DAC **10b** in such outer loop(s) alleviates this problem, since they feed back the lowest average current and thereby gives the optimum thermal noise performance and clock jitter sensitivity. In combination, these measures provide reduced requirements on the gain bandwidth of the integrating amplifiers of the innermost loop and the best noise performance of the outermost loop. The present invention therefore facilitates increased sampling rates giving either increased bandwidth or dynamic range of the $\Delta\Sigma$ -ADC at a low cost. Alternatively, the reduced sensitivity to loop delay can be utilized to reduce the power consumption by reducing the excess bandwidth of the integrating amplifiers commonly introduced to guarantee stability in presence of process variations and mismatch.

Accordingly, in some embodiments of the present invention, the first DAC **10a** is located in a first feedback loop and the second DAC **10b** is located in a second feedback loop, which is an outer feedback loop relative to the first feedback loop (i.e., which has a higher order of integration than the first feedback loop). For example, the first loop may be the innermost loop, i.e. a loop with first order integration. Furthermore, the second loop may be the outermost loop, i.e. the loop with the highest order integration.

Even though the timing of the feedback pulses can be chosen arbitrary in principle there are practical restrictions coming from the time required to avoid quantizer metastability, and the complexity of the clocking scheme.

The decision time of the quantizer requires us to choose the start point of all feedback pulses significantly after the quantizer sampling instant nT ($nT \ll (n+\alpha_k)T$ for all k, for example $\alpha_k > 0.1$). The exact timing depends on the clocking scheme. For a two phase (0, 180 degree) clocking scheme, a natural starting point (i.e. $(n+\alpha_k)T$) is $(n+0.5)T$, while if a four phase clocking scheme is available, $(n+0.25)T$ may be chosen, and eight phases would facilitate a starting point of $(n+0.125)T$.

While the inventors have not found any particular advantage of having different starting points for different feedback pulses, the selection of the endpoint on the other hand, has been found to influence the sensitivity to clock jitter and loop delay, as well as the thermal noise performance of the DAC. It yields the best noise performance to maximize the relative feedback pulse duration $(\beta-\alpha)$. Therefore, according to some embodiments, in the outermost loops, which contribute a lot to the overall noise performance of the $\Delta\Sigma$ -ADC, $(\beta-\alpha)=1$ is chosen. Thus, depending on the available clock scheme, natural end points for the outermost loops would be $(n+\beta_2)T=(n+1+0.5)T$, $(n+1+0.25)T$ or $(n+1+0.125)T$. The inventors have further found that the sensitivity to loop delay is reduced if the innermost DAC pulse end point is significantly earlier than the succeeding quantizer sampling instant, i.e. $\beta_1 \ll 1$, for example $\beta_1 < 0.9$. A convenient choice for most RZ (return to zero) clocking schemes is to have 50% duty cycle for the innermost feedback pulses, resulting in end points of $(n+\beta_1)T=(n+0.5+0.5)T$, $(n+0.5+0.25)T$ or $(n+0.5+0.125)T$, depending on the clock scheme. An important remark here is of course that $(n+0.5+0.5)T$ equals the timing of the succeeding sampling instant and therefore yields no improved sensitivity to loop delay. Thus, at least a four phase clocking scheme is needed.

Alternatively, when any clocking scheme is used, arbitrary starting points may be accomplished by using delay elements, such as an inverter or a plurality of cascaded inverters (depending on what delay is desired) to generate delayed clock pulses of other delays than those naturally provided by the clock phases of a particular clocking scheme (e.g. four-phase or eight phase). However, such a delay would have to be relatively exact, or well defined, in order not to change the transfer function of the loop, and it is typically easier to get a high precision in the clock delay by using the already well defined clock phases naturally provided by the particular clocking scheme.

The inventors have realized that a DAC, which is used for feedback in a continuous-time $\Delta\Sigma$ -ADC, can be advantageously implemented using two switched capacitor DACs (as subcomponents) that share a common output and operate on the same input but with a mutual delay in time. Hence, the two switched-capacitor DACs (subcomponents) are thus arranged to together act as a single combined DAC, which is different from e.g. two switched-capacitor DACs that have separate individual outputs and/or are arranged to operate on different inputs. Hence, according to some embodiments of the present invention, at least one DAC of the two or more DACs **10a-b** comprises two switched-capacitor (SC) DACs (as sub components). Embodiments of such DACs are illustrated in FIGS. **8-9**. In FIGS. **8-9**, a first one of the SC DACs is labeled **40** and a second one of the SC DACs is labeled **50**. For each n, each of the two switched capacitor DACs **40** and **50** is arranged to be charged with a charge proportional to the corresponding sample $y(n)$ of the digital output signal. The first SC DAC **40** is arranged to be switched in to the continuous-time analog

network **20** for transfer of its charge to the continuous-time analog network **20** in a time interval that lasts between the time instants $(n+\alpha_3)T$ and $(n+\beta_3)T$. Furthermore, the second SC DAC **50** is arranged to be switched in to the continuous-time analog network **20** for transfer of its charge to the continuous-time analog network **20** in a time interval that lasts between the time instants $(n+\alpha_4)T$ and $(n+\beta_4)T$. These parameters are related such that $\beta_4 > 1$, $0 < \alpha_3 < \alpha_4 < \beta_4 < 2$ and $\alpha_3 < \alpha_4 \leq 1$. This is schematically illustrated with a waveform diagram in FIG. 10, further discussed below.

According to some embodiments, the aforementioned DAC comprising the two SC DACs (as subcomponents) is the second DAC **10b** (in which case $\alpha_3 = \alpha_2$ and $(\beta_4 = \beta_2)$), as is also indicated with reference signs **10b** used in FIGS. 8-9. However, this use of reference signs should not be seen as limiting. Additionally or alternatively, in other embodiments, one or more other DACs may be implemented using two SC DACs (as subcomponents).

In some embodiments, the DAC comprising the two SC DACs is located in a feedback loop, which is an outer feedback loop (i.e. a feedback loop of higher order) relative to the first feedback loop.

In the SC feedback according to FIG. 1 discussed in the background, a capacitor C_{REF} is switched using a set of switches between the reference voltage V_{REF} and to the inverting input of the operational amplifier. A reference resistance R_{REF} might be connected on either side of the capacitor to lower the time constant of the switching RC circuit. The reference capacitor is charged with the reference voltage (V_{REF+} or V_{REF-}) corresponding to the digital output bit (single-bit quantization is assumed) in a first clock phase, and then transfers a well defined charge packet $Q = C \cdot V_{REF}$ to the integrator in a second clock phase when the switch circuit switches the reference capacitor C_{REF} to the inverting input of the amplifier. The discharge of the capacitor C_{REF} will give an exponentially falling current pulse $\tau = I_0 \cdot \exp(-t/\tau)$ where $\tau = R_{REF} \cdot C_{REF}$ is the time constant. Because of the exponentially decreasing pulse shape the charge Q displaced in one clock cycle T varies only slightly when clock jitter occurs, and thus this technique is less sensitive to clock jitter than the $\Delta\Sigma$ ADCs illustrated in FIGS. 1-2. Furthermore, an advantage of using two switched capacitor DACs with mutually displaced output pulses has the advantage, compared with a single switched-capacitor DAC, that the peak current is reduced, whereby the risk of slewrates limitations in the continuous-time analog network **20** is reduced. This can e.g. be exploited by implementing the continuous-time analog network **20** using components with less harsh slewrates requirements, which in turn enables a reduced current consumption.

FIG. 8 shows a 1-bit version of the DAC comprising the two SC DACs **40-50** according to an embodiment. Each SC DAC **40** and **50** comprises a capacitor and a set of switches as depicted in FIG. 8. Switches of the SC DACs **40** and **50** are controlled by non-overlapping switch phases s_3 - s_4 and s_5 - s_6 , respectively. Below, the output bit of the quantizer **5** is assumed to be 1. If it is 0, then V shall be replaced by $-V$ in the following discussion. When s_3 is on (conducting) the first of the switched capacitor DACs **40** is charging to $Q = V \cdot C/2$. When s_4 is on the first of the switched capacitor DACs **40** is discharging into the analog network **20**. For proper operation s_3 and s_4 should not be on at the same time. When s_5 is on the second of the switched capacitor DACs **50** is charging to $Q = V \cdot C/2$. When s_6 is on the second of the switched capacitor DACs **50** is discharging into the analog network **20**. For proper operation s_5 and s_6 should not be on at the same time.

A resistor (with resistance $2R$) is connected in series with each one of the switched capacitors to control the time con-

stant (RC) of its discharge and the peak of the output current $I = V/(2R)$. In FIG. 9, the two SC DACs **40** and **50** are implemented as in FIG. 8. However, in FIG. 9, a shared resistor (with resistance $2R$) is used for the two SC DACs **40** and **50**.

For someone skilled in the art it is straightforward to extend the 1-bit switched capacitor DACs shown in FIGS. 8 and 9 into multi-bit switched capacitor DACs by using e.g. binary weighted or thermometer coded switched capacitor banks controlled in the same way (for embodiments where the quantizer **5** is a multibit quantizer).

The first **40** and the second **50** SC DAC together generate an overall DAC impulse response as exemplified in FIG. 10. Generally, the two discharge time intervals of the first **40** and second **50** of the switched capacitor DACs can be chosen arbitrary. In FIG. 10, they have been illustrated for $\beta_3 < \alpha_4$ for ease of illustration. However, in other embodiments these parameters may be such that $\beta_3 > \alpha_4$ or $\beta_3 = \alpha_4$ as well. The inventors have found that having $\beta_3 = \alpha_4$ typically yields the best or close to the best implementation in practice. Also, it seems practical to have the same capacitor size in the first **40** and the second **50** of the switched capacitor DACs (letting them carry half of the charge from each of the sampling instants nT each), as shown in FIG. 8 and FIG. 9, even though any other ratio between the capacitor sizes could be used in principle. Having equal capacitor size also gives the same discharge time constants for the two segments of the impulse response.

Using a two-phase (0 and 180 degrees) clock scheme can yield the following timing of the feedback pulses: $\alpha_3 = 0.5$, $(\beta_3 = \alpha_4 = 1)$, and $\beta_4 = 1.5$. Since the charging of the switched capacitor DACs will take place from $(n-1+\beta_3)T$ to $(n+\alpha_3)T$ and $(n-1+\beta_4)T$ to $(n+\alpha_4)T$ the first of the switched capacitor DACs **40** will charge with a charge proportional to the sample of the digital output signal at sample instant nT in the same time interval as the second of the switched capacitor DACs **50** is discharging its charge proportional to the sample of the digital output signal at the preceding sample instant $(n-1)T$.

Using a four-phase (0, 90, 180, and 270 degrees) clock scheme could e.g. yield the following timing of the feedback pulses: $\alpha_3 = 0.25$, $\beta_3 = \alpha_4 = 1$, and $\beta_4 = 1.75$. Since the sum of the discharge time intervals of the first and second of the switched capacitor DACs **40** is greater than the sampling interval T , there will be some overlap between the discharge time intervals of the first and second of the switched capacitor DACs **50**, in this case from $(n+0.25)T$ to $(n+0.75)T$, for all n .

When the discharge time intervals of the first and second of the switched capacitor DACs is not overlapping, as is the case for the two-phase clock scheme above, the series resistor can be shared between the first **40** and second **50** of the switched capacitor DACs, as shown in FIG. 9.

According to some embodiments, a radio receiver circuit comprises the continuous-time $\Delta\Sigma$ -ADC **1**. This is schematically illustrated in FIG. 11, where the continuous-time $\Delta\Sigma$ -ADC **1** is placed in a radio receiver circuit **100** in between the analog signal processing domain (circuits to the left of the $\Delta\Sigma$ -ADC **1**) and the digital signal processing domain (block marked DSP).

According to some embodiments, an integrated circuit comprises the continuous-time $\Delta\Sigma$ -ADC **1**. This is schematically illustrated in FIG. 12, where the continuous-time $\Delta\Sigma$ -ADC **1** is placed in an integrated circuit (IC) **200**.

In some embodiments, a radio communication apparatus comprises the continuous-time $\Delta\Sigma$ -ADC **1**. For example, the radio communication apparatus may comprise a radio receiver circuit, such as the radio receiver circuit **100** and/or an integrated circuit, such as the integrated circuit **200**, that in turn comprises the $\Delta\Sigma$ -ADC **1**.

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Non-limiting examples of such radio communication apparatuses are a mobile phone, a wireless data modem, and a radio base station. FIG. 13 schematically illustrates examples of radio communication apparatuses in the form of a mobile phone 300 and a radio base station 400 in communication with each other.

The present invention has been described above with reference to specific embodiments. However, other embodiments than the above described are possible within the scope of the invention. For example, in addition to the types of DACs described, other types of DACs, e.g. using other pulse durations, may be used as well for some of the two or more DACs. The different features of the embodiments may be combined in other combinations than those described. The scope of the invention is only limited by the appended patent claims.

The invention claimed is:

1. A continuous-time delta-sigma ($\Delta\Sigma$) analog-to-digital converter (ADC) comprising:

a sampled quantizer arranged to generate samples $y(n)$ of a digital output signal of the $\Delta\Sigma$ -ADC at sample instants nT , where n is an integer sequence index and T is a sampling period, based on an analog input signal to the quantizer;

two or more digital-to-analog converters (DACs), each arranged to generate an analog feedback signal based on the samples of the digital output signal generated by the sampled quantizer; and

a continuous-time analog network arranged to generate the analog input signal to the quantizer based on the feedback signals from the two or more DACs and an analog input signal to the $\Delta\Sigma$ -ADC;

wherein:

at least a first DAC of the two or more DACs is adapted to generate a pulsed feedback signal that, for each n , comprises a pulse, the magnitude of which is proportional to the sample of the digital output signal at sample instant nT and which lasts between the time instants $(n+\alpha_1)T$ and $(n+\beta_1)T$, wherein $0<\alpha_1<\beta_1<1$;

at least a second DAC of the two or more DACs is adapted to generate a pulsed feedback signal that, for each n , comprises a pulse, the magnitude of which is proportional to the sample of the digital output signal at sample instant nT and which lasts between the time instants $(n+\alpha_2)T$ and $(n+\beta_2)T$, wherein $0<\alpha_2<1<\beta_2$; and

the first DAC is located in a first feedback loop and the second DAC is located in a second feedback loop, which is an outer feedback loop relative to the first feedback loop.

2. The continuous-time $\Delta\Sigma$ -ADC according to claim 1, wherein $\beta_1<0.9$.

3. The continuous-time $\Delta\Sigma$ -ADC according to claim 2, wherein $\beta_1=0.625$.

4. The continuous-time $\Delta\Sigma$ -ADC according to claim 2, wherein $\beta_1=0.75$.

5. The continuous-time $\Delta\Sigma$ -ADC according to claim 1, wherein $\alpha_1>0.1$.

6. The continuous-time $\Delta\Sigma$ -ADC according to claim 5, wherein $\alpha_1=0.125$.

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7. The continuous-time $\Delta\Sigma$ -ADC according to claim 5, wherein $\alpha_1=0.25$.

8. The continuous-time $\Delta\Sigma$ -ADC according to claim 1, wherein $\beta_2-\alpha_2=1$.

9. The continuous-time $\Delta\Sigma$ -ADC according to claim 1, wherein at least one DAC of the two or more DACs comprises two switched-capacitor DACs, wherein, for each n :

each of the two switched capacitor DACs is arranged to be charged with a charge proportional to the corresponding sample $y(n)$ of the digital output signal;

a first of the switched capacitor DACs is arranged to be switched in to the continuous-time analog network for transfer of its charge to the continuous-time analog network in a time interval that lasts between the time instants $(n+\alpha_3)T$ and $(n+\beta_3)T$; and

a second of the switched capacitor DACs is arranged to be switched in to the continuous-time analog network for transfer of its charge to the continuous-time analog network in a time interval that lasts between the time instants $(n+\alpha_4)T$ and $(n+\beta_4)T$;

wherein $\beta_4>1$, $0<\alpha_3<\alpha_4<\beta_4<2$ and $\alpha_3<\beta_3\leq 1$.

10. The continuous-time $\Delta\Sigma$ -ADC (1) according to claim 9, wherein the first DAC is located in a first feedback loop and the DAC comprising the two switched capacitor DACs is located in another feedback loop, which is an outer feedback loop relative to the first feedback loop.

11. The continuous-time $\Delta\Sigma$ -ADC according to claim 10, wherein the second DAC is the DAC that comprises the two switched-capacitor DACs.

12. The continuous-time $\Delta\Sigma$ -ADC according to claim 1, wherein the continuous-time analog network comprises a plurality of cascaded continuous-time integrators.

13. The continuous-time $\Delta\Sigma$ -ADC according to claim 12, wherein

a first one of the integrators is arranged to receive a feedback signal from one of the DACs, connected to the first integrator, and the analog input signal of the $\Delta\Sigma$ -ADC as input signals; and

each of the other integrators is arranged to receive a feedback signal from one of the DACs, connected to that integrator, and an output signal of a preceding integrator as input signals.

14. The continuous-time $\Delta\Sigma$ -ADC according to claim 12, wherein a last one of the cascaded continuous-time integrators is arranged to generate the analog input signal to the sampled quantizer.

15. The continuous-time $\Delta\Sigma$ -ADC according to claim 1, wherein the continuous-time $\Delta\Sigma$ -ADC is comprised in a radio receiver circuit, where the analog input signal to the $\Delta\Sigma$ -ADC is a received radio signal or is derived from the received radio signal.

16. The continuous-time $\Delta\Sigma$ -ADC according to claim 1, wherein the continuous-time $\Delta\Sigma$ -ADC is comprised in an integrated circuit.

17. The continuous-time $\Delta\Sigma$ -ADC according to claim 1, wherein the continuous-time $\Delta\Sigma$ -ADC is comprised in a radio communication apparatus comprising one of: a mobile phone, a wireless data modem, or a radio base station.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 9,118,344 B2
APPLICATION NO. : 14/355651
DATED : August 25, 2015
INVENTOR(S) : Anderson et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On The Title Page,

In Item (57), under “ABSTRACT”, in Column 2, Line 15, delete “ $(n+a1)T$ and $(\eta+\beta1)$ ” and insert -- $(n+\alpha1)T$ and $(n+\beta1)$ --, therefor.

In Item (57), under “ABSTRACT”, in Column 2, Line 16, delete “ Af ” and insert -- At --, therefor.

In Item (57), under “ABSTRACT”, in Column 2, Line 21, delete “ $(n+a2)T$ and $(\eta+\beta2)T$, wherein $0<a2<1<\beta2$.” and insert -- $(n+\alpha2)T$ and $(n+\beta2)T$, wherein $0<\alpha2<1<\beta2$. --, therefor.

In The Specification

In Column 2, Line 52, delete “ $(n+\approx1)T$,” and insert -- $(n+\beta1)T$, --, therefor.

In Column 7, Line 9, delete “ $\alpha3<\alpha3\leq1$.” and insert -- $\alpha3<\beta3\leq1$. --, therefor.

In Column 7, Line 13, delete “ $(\beta4=\beta2)$,” and insert -- $\beta4=\beta2$, --, therefor.

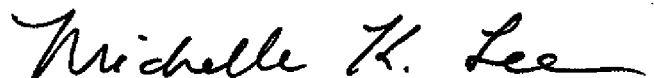
In Column 8, Line 30, delete “ $(\beta3=\alpha4=1)$,” and insert -- $\beta3=\alpha4=1$, --, therefor.

In The Claims

In Column 9, Line 18, in Claim 1, delete “ (As) ” and insert -- $(\Delta\Sigma)$ --, therefor.

In Column 10, Line 23, in Claim 10, delete “ $\Delta\Sigma\text{-ADC}(1)$ ” and insert -- $\Delta\Sigma\text{-ADC}$ --, therefor.

Signed and Sealed this
Eighth Day of March, 2016



Michelle K. Lee
Director of the United States Patent and Trademark Office